REMARKS

This application has been revised and the following remarks are submitted in light of the Office Action mailed November 4, 2004. Claims 1-16 are presented for examination. Claims 1 and 12-14 have been amended.

The claim amendments and new claims presented herein are fully supported by the specification as originally filed. Claims 1, 12 and 13 as amended are supported by the specification at paragraphs [0014] and [0015], and Claim 14 as amended is supported at paragraph [0026]. In addition, the title has been replaced with a new title, and paragraphs [0015], [0023] and [0028] have been amended to reflect changes made to the drawings. No new matter has been added.

Objection to the Title

The title is objected to because it is found to be not descriptive. The title has been replaced with a new title which is believed to be indicative of the claimed invention. Applicants therefore submit that this objection to the title has been overcome. If the Examiner has any further objection to the title, a suggested substitute title is invited.

Objection to the Drawings under 37 C.F.R. 1.83(a)

The drawings are objected to under 37 C.F.R. 1.83(a) because the drawings are found to lack "a plurality of integrated circuits" and "a dicing channel disposed between adjacent ones of said integrated circuits", as recited in Claim 1. Each of Figures 1 and 2 have been amended to show more than one integrated circuit chip 11 and a dicing channel 18 between each chip. With regard to Claim 14, Applicants respectfully submit that conductors 14 are shown as being jogged (see specification at paragraph [0015]). Replacement drawings sheets 1 and 2 are submitted herewith. Applicants therefore submit that this objection to the drawings has been overcome.

Rejection of Claims 1-16 under 35 U.S.C. 112, second paragraph

Claims 1-16 are rejected under 35 U.S.C. 112, second paragraph as being indefinite. Applicants respectfully traverse this rejection.

In Claim 1, the features "a plurality of integrated circuits" and "a dicing channel disposed between adjacent ones of said integrated circuits" are found to be unclear and confusing. As discussed above, each of Figures 1 and 2 have been amended to show more than one integrated circuit chip 11 and a dicing channel 18 between adjacent ones of the integrated circuit chips. Applicants therefore submit that Claim 1, when read in light of the specification and drawings, is not indefinite.

In Claim 14, the feature "said conductors are S-shaped or spring shaped or jogged" is found to be unclear and confusing. Initially, Applicants note that Claim 14 has been amended to recite that "said conductors are jogged." Applicants respectfully submit that the figures show conductors 14 as being jogged (see specification at paragraph [0015]), and therefore submit that Claim 14, when read in light of the specification and drawings, is not indefinite.

Accordingly, Applicants respectfully submit that Claims 1-16 meet the requirements of 35 U.S.C. 112, second paragraph, and therefore request withdrawal of this rejection.

Rejection of Claims 1-8 and 10-12 under 35 U.S.C. 102(b) over Yerman

Claims 1-8 and 10-12 are rejected under 35 U.S.C. 102(b) over U.S. Patent No. 4,017,340 to Yerman. Applicants respectfully traverse this rejection.

Claim 1 is directed to a semiconductor wafer comprising a substrate, a plurality of integrated circuit chips fabricated on a substrate, a dicing channel disposed between the chips, a layer of a first material on a top surface and sidewalls of the chips, and at least one layer of a second dielectric material on the layer of first dielectric material. Thus, it is a feature of the present invention that the semiconductor wafer comprises a plurality of chips fabricated on a substrate, and it is a further feature that a layer of first dielectric material is disposed on a top surface and sidewalls of the chips.

Applicants respectfully submit that these features (at least) are not disclosed by Yerman, as follows.

The Yerman patent is directed to a semiconductor element having a polymeric protective coating and a glass coating overlay. The semiconductor element 10 comprising body 12, as shown in Figure 1, is a single semiconductor device such as a transistor, rather than an integrated circuit chip. Moreover, only one semiconductor element 10 is shown by Yerman, rather than a plurality of devices. Yerman therefore fails to disclose a plurality of integrated circuit chips fabricated on a substrate.

Yerman also discloses that the polymeric protective coating 46 is disposed only on the sidewalls of semiconductor element 10. Yerman therefore fails to disclose a layer of first dielectric material disposed on a top surface and sidewalls of integrated circuit chips.

Since Yerman fails to disclose each and every element of the claimed invention, Applicants respectfully submit that Claim 1 is not anticipated by Yerman. Claims 2-8 and 10-12, which depend from Claim 1, also are not anticipated by Yerman. Applicants therefore request withdrawal of this rejection.

Rejection of Claims 13-16 under 35 U.S.C. 103(a) over Yerman

Claims 13-16 are rejected under 35 U.S.C. 103(a) over Yerman. Applicants respectfully traverse this rejection.

Claims 13-16 each depend ultimately from Claim 1. As discussed previously, it is a feature of the present invention that the semiconductor wafer comprises a plurality of chips fabricated on a substrate, and it is a further feature that a layer of first dielectric material is disposed on a top surface and sidewalls of the chips. Applicants respectfully submit that these features (at least) are neither disclosed nor suggested by Yerman, as follows.

By disclosing only a single semiconductor device 10, Yerman fails to disclose a plurality of integrated circuit chips fabricated on a substrate. And by disclosing that the polymeric protective coating 46 is disposed only on the sidewalls of

semiconductor element 10, Yerman fails to disclose a layer of first dielectric material disposed on a top surface and sidewalls of integrated circuit chips.

Yerman also fails to suggest these features of the present invention. The present invention is directed to protecting weak back-end-of-line interconnects from the harsh external environment and stresses associated with assembly and packaging. In contrast, the Yerman patent is directed to a multilayer passivation-encapsulation for a single semiconductor element. Yerman's disclosure of a single semiconductor element provides no suggestion of a plurality of integrated circuit chips fabricated on a substrate.

Moreover, the Yerman invention addresses the need for a passivation coating capable of providing a charge neutral surface on P-N junctions of such devices. For this reason, polymeric protective coating 46 is disposed only on sidewall 36 of semiconductor element 10, and particularly on P-N junctions 28 and 30. Yerman has no reason to provide a passivation coating on the top surface of semiconductor element 10, and therefore provides no suggestion of a layer of first dielectric material disposed on a top surface and sidewalls of a plurality of integrated circuit chips.

Accordingly, Applicants respectfully submit that Claim 1 is patentable over Yerman. Claims 13-16, which depend from Claim 1, also are patentable over Yerman. Applicants therefore request withdrawal of this rejection.

Claims 13 and 14 are also patentable over Yerman for the following additional reason. It is a feature of Claim 13 that a plurality of conductors is embedded in the first dielectric material and the second dielectric material. Yerman fails to disclose or even suggest a plurality of conductors embedded in protective coating 46 and glass layer 48. Accordingly, Applicants respectfully submit that Claim 13 is patentable over Yerman. Claim 14, which depends from Claim 13, is also patentable over Yerman. For this additional reason, Applicants therefore request withdrawal of the rejection of these claims.

Rejection of Claim 9 under 35 U.S.C. 103(a) over Yerman in view of Sun et al.

Claim 9 is rejected under 35 U.S.C. 103(a) over Yerman in view of Sun et al. Applicants respectfully traverse this rejection.

Claim 9 depends from Claim 1. As discussed previously, it is a feature of the present invention that the semiconductor wafer comprises a plurality of chips fabricated on a substrate, and it is a further feature that at least two layers of dielectric material are disposed on a top surface and sidewalls of the chips. Applicants respectfully submit that these features (at least) are neither disclosed nor suggested by Yerman, as follows.

By disclosing only a single semiconductor device 10, Yerman fails to disclose or even suggest a plurality of integrated circuit chips fabricated on a substrate. And by disclosing that the polymeric protective coating 46 and glass layer 48 are disposed only on the sidewalls of semiconductor element 10, Yerman fails to disclose or even suggest at least two layers of dielectric material disposed on a top surface and sidewalls of integrated circuit chips.

Sun et al. fail to remedy the deficiencies of the Yerman disclosure in this regard. The Sun et al. patent is directed to a passivation process over a memory link. Sun et al. disclose passivation of a single memory link, and therefore fail to disclose or even suggest a plurality of integrated circuit chips fabricated on a substrate and at least two layers of dielectric material disposed on a top surface and sidewalls of integrated circuit chips.

Accordingly, Applicants respectfully submit that Claim 1 is patentable over Yerman in view of Sun et al. Claim 9, which depends from Claim 1, is also patentable over Yerman in view of Sun et al. Applicants therefore request withdrawal of this rejection.

Conclusion

Applicants have properly traversed each of the grounds for rejection in the Office Action, and therefore submit that the present application is now in condition for allowance. If the Examiner has any questions or believes further discussion will aid examination and advance prosecution of the application, a telephone call to the undersigned is invited.

No fee is believed to be due for the submission of this amendment. If any fees are required, however, the Commissioner is authorized to charge such fees to Deposit Account No. 09-0458.

Respectfully Submitted,

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